Massively Parallel and Sliced Optical Network

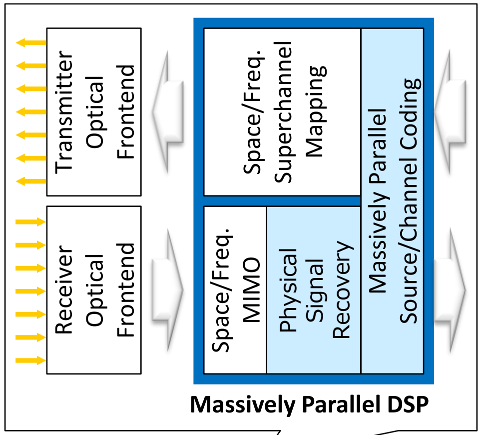
Commissioned Research (#204) of NICT, Japan

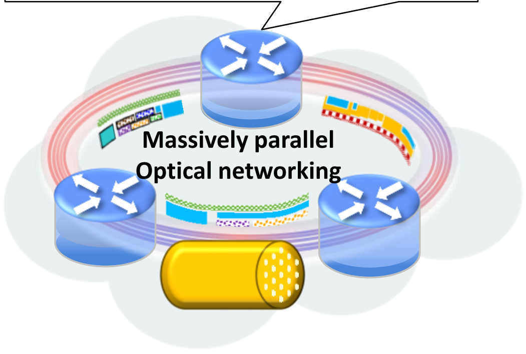
MAPLE
Massively Parallel and Sliced Optical Network

Project overview

Aim: to establish a novel optical network supporting future large-scale/diverse traffic streams

This work: to develop fundamental technologies with massively-parallel processing for low-consumption, open, and versatile optical transport





Member institutions

MITSUBISHI ELECTRIC
Changes for the Better

AIST

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Keio University
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1. Massively Parallel Advanced DSP Technology

MITSUBISHI ELECTRIC
Changes for the Better

1.A: Signal recovery and adaptive control

- **Final Goal:** Based on the premise of evolving semiconductor processes and logic circuit technology (expected to increase capacity by a factor of 4.2) enabling implementation by around 2030, we will increase the current transmission capacity of 1 Tbps by 10 times to 10 Tbps, and establish a fundamental technology that also enables a 25-fold increase in power efficiency. The system configuration and algorithms alone will achieve a six-fold improvement in power efficiency.

- **Progress:** (1) Developed several methods to achieve high capacity and low power consumption. (2) Key technologies were implemented in FPGAs for high-throughput verification. Various transmission evaluations of 400 Gb/s per wavelength and experiments in collaboration with 1.B were conducted. (3) Presented the R&D results to the Ministry of Internal Affairs and Communications commissioned research framework that runs parallel to the project.

- **Results:** (1) Improved the power efficiency of soft-decision error correction by 8 to 26 times with compressed shaping (CS)-multilevel coding (MLC) 256-QAM, compared with bit-interleaved coded uniform 128-QAM (Fig. 1.A-1). (2) Achieved throughput > 2 Tb/s or up to 2^{22}-QAM shaping based on hierarchical subcarrier rate and distribution matching in a single FPGA (Fig. 1.A-2). Performed probabilistically shaped 400 Gb/s/λ transmission over a 7-node 500 km-class fiber link and 220 m of free space with a record capacity of 14 Tb/s. Combined with 1.B, achieved both better transmission performance and power efficiency when coding with a CS-MLC-64-QAM signal (Fig. 1.A-3).

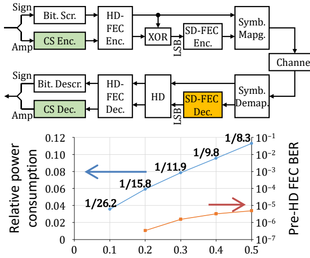
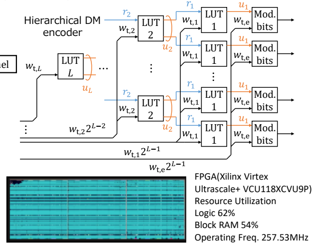
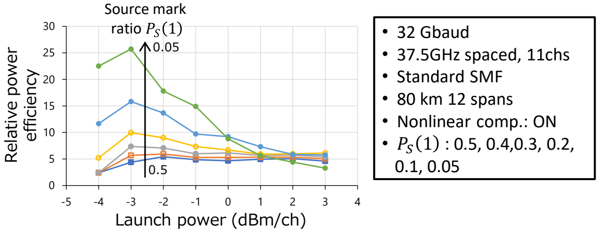


Fig. 1.A-1: CS-MLCM configuration and power consumption



FPGA(Xilinx Virtex Ultrascale+ VCU118XCVU9P)
Resource Utilization
Logic 62%
Block RAM 54%
Operating Freq. 257.53MHz

Fig. 1.A-2: FPGA implementation at >2 Tb/s throughput



- 32 Gbaud
- 37.5GHz spaced, 11chs
- Standard SMF
- 80 km 12 spans
- Nonlinear comp.: ON
- $P_S(1)$: 0.5, 0.4,0.3, 0.2, 0.1, 0.05

Fig. 1.A-3: Relative power consumption (co-simulation with 1.B)

AIST

1.B:Optical transmission/ reception processing

- **Final Goal:** Development of a signal processing technique to compensate for the nonlinear waveform distortion of wavelength-division multiplexed (WDM), high-order QAM signals with a spectral efficiency of more than 10bit/s/Hz after long-distance transmission based on an artificial neural network (ANN). The objective is to increase transmission distance by 60% (+2dB) compared with a case with no nonlinearity compensation.

- **Progress:** A physics-based ANN to compensate for nonlinear waveform distortion of WDM signals considering cross-phase modulation (XPM) as well as self-phase modulation (SPM) has been proposed, and its effectiveness has been confirmed by numerical simulation and a transmission experiment employing offline digital signal processing.

- **Results:** We evaluated by numerical simulation the quality of 9-channel, 32Gbaud DP-64QAM signals after transmission across a line consisting of multiple spans of 80-km SSMF, and confirmed that the proposed scheme could increase the distance by 60%.

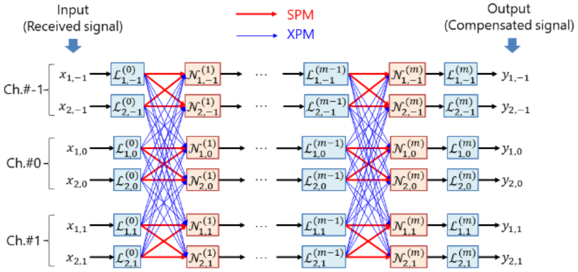


Fig. 1.B-1: Block diagram of proposed physics-based ANN to calculate back propagation of WDM signals considering both XPM and SPM.

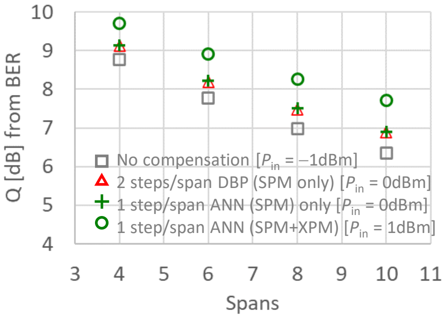


Fig. 1.B-2: Quality of 9ch DP-64QAM signals versus transmission distance obtained by numerical simulation.

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2. Massively Parallel Optical Networking Technology

2.A: Design and control for massively sliced optical networks

KDDI Research

- **Final Goal:** In this project, we will develop (1) efficient slice (optical channel) design technology for three axes, which are the conventional frequency axis and two space-multiplexed axes (mode and core), and (2) control technology for complex slices with three degrees of freedom (frequency, core and mode).

- **Progress:** We constructed a testbed and verified the slice control using an open control interface based on basic verification of signal parallelism equivalent to 1000 times the current level (6 times the mode groups, 9 times the wavelengths, 19 times the cores, and 80 wavelengths of current single mode) and monitoring for major quality degradation factors between slices. In addition, controllability was verified by extending the data model of the open control interface by considering the cores, modes, and frequencies.

- **Results:** We have established a massively parallel optical network design technology that makes full use of the spatial/frequency multiplexing axes to achieve 1000 times the current level of optical signal parallelism, and a slice control technology that utilizes an open control interface. In addition, the verification of the basic technology equivalent to 1000 times the parallelism and 100 times the expansion/contraction was completed in collaboration within Group 2.

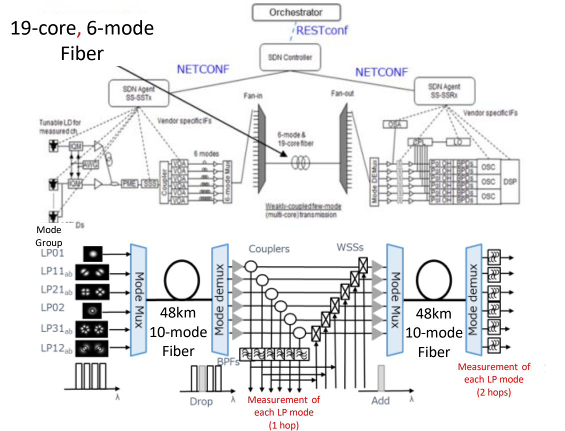


Fig. 2.A-1. Testbed for massively parallel slice control verification using open control interface

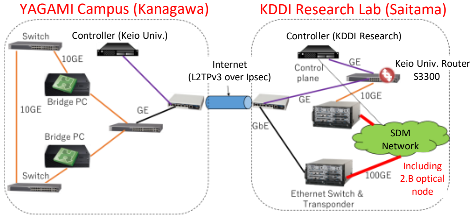


Fig. 2.A-2. Testbed for collaboration within Group 2

2.B: Massively parallel optical node and network architectures

KAGAWA UNIVERSITY

- **Final Goal:** To establish a massively parallel optical node and network configuration technology that makes it possible to achieve expansion and contraction 100 times greater than that with the current technology by making full use of the space/frequency axis.

- **Progress:** Various methods for configuring spatial cross connect (SXC) based on core selective switches (CSS) were investigated and evaluated. We also devised and implemented WDM/SDM multilayer routing calculation and core/frequency slot assignment algorithms, constructed a hierarchical optical node demonstration testbed for "Few-mode" Fiber (FMF), and performed an analysis with ASE noise and nonlinear noise.

- **Results:** We demonstrated that an SXC based on CSS can reduce the hardware compared to a conventional configuration based on fiber switches. We also demonstrated that it is possible to configure and switch optical channels with 100 times more elasticity (from 100 Gb/s to 40 Tb/s) than with the current configuration, thus achieving the numerical target. Collaboration within Group 2 demonstrated the feasibility of a hierarchical optical node architecture capable of accommodating FMFs with mixed weak and strong coupling.

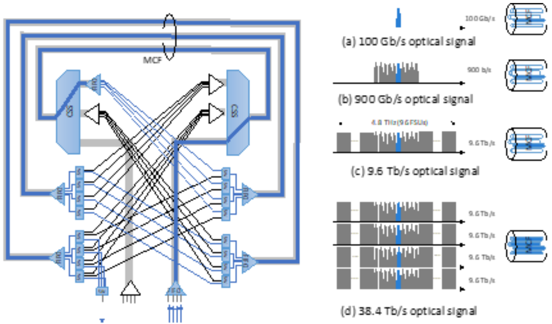


Fig. 2.B-1: Demonstration test setup for establishing a stretchable optical channel

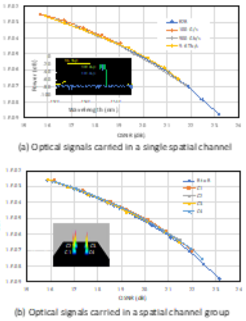


Fig. 2.B-2: Experimental results

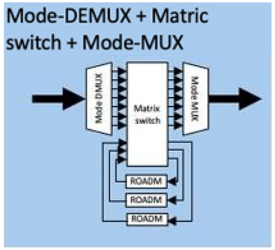


Fig. 2.B-3: Optical node architecture used for collaborative experiment

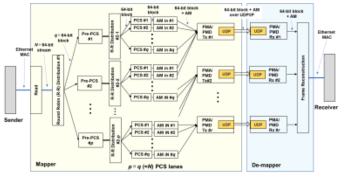
2.C: Dynamic MAC

Keio University

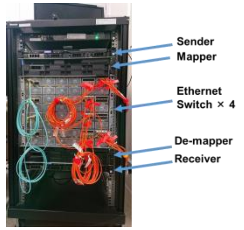
- **Final Goal:** To realize large-scale optical networking based on 100-SDM and 10-Tb/s class super-channel, we will establish the basic MAC technology using a dynamic MAC emulator that can dynamically change the bandwidth.

- **Progress:** We devised a dynamic MAC architecture with 400 lanes, and investigated methods for (1) bandwidth scaling, (2) skew compensation, and (3) partial failure handling by the dynamic MAC. We built an emulator in software based on this architecture, and verified the operation of the basic functions of bandwidth expansion/contraction, skew compensation, and lane fault handling both in the laboratory and in a wide area environment using the Japan Gigabit Network (JGN).

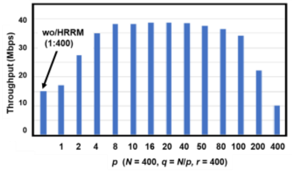
- **Results:** (1) A multi-stage round-robin scheme was devised and its effectiveness was confirmed from throughput improvement on a dynamic MAC emulator (Fig. 2.C-1). In addition, the feasibility of 400 lanes was confirmed using the emulator. (2) Demonstrated the feasibility of 5 ms skew compensation through the JGN and in collaborative experiments (Fig. 2.C-2). (3) The basic operation of the automatic recovery mechanism for lane failures was confirmed using the emulator (Fig. 2.C-3).



(a) Dynamic MAC Functional Diagram

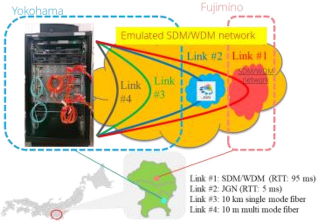


(b) Dynamic MAC emulator



(c) 400 lane throughput measurement on dynamic MAC emulator

Fig. 2.C-1: Implementation and evaluation of dynamic MAC emulator



Link #1: SDM/WDM (RTT: 95 ms)
Link #2: JGN (RTT: 5 ms)
Link #3: 10 km single mode fiber
Link #4: 10 m multi mode fiber

Fig. 2.C-2: Collaborative experimental setup

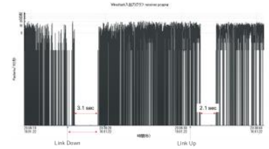


Fig. 2.C-3: Experimental results for automatic recovery mechanism