

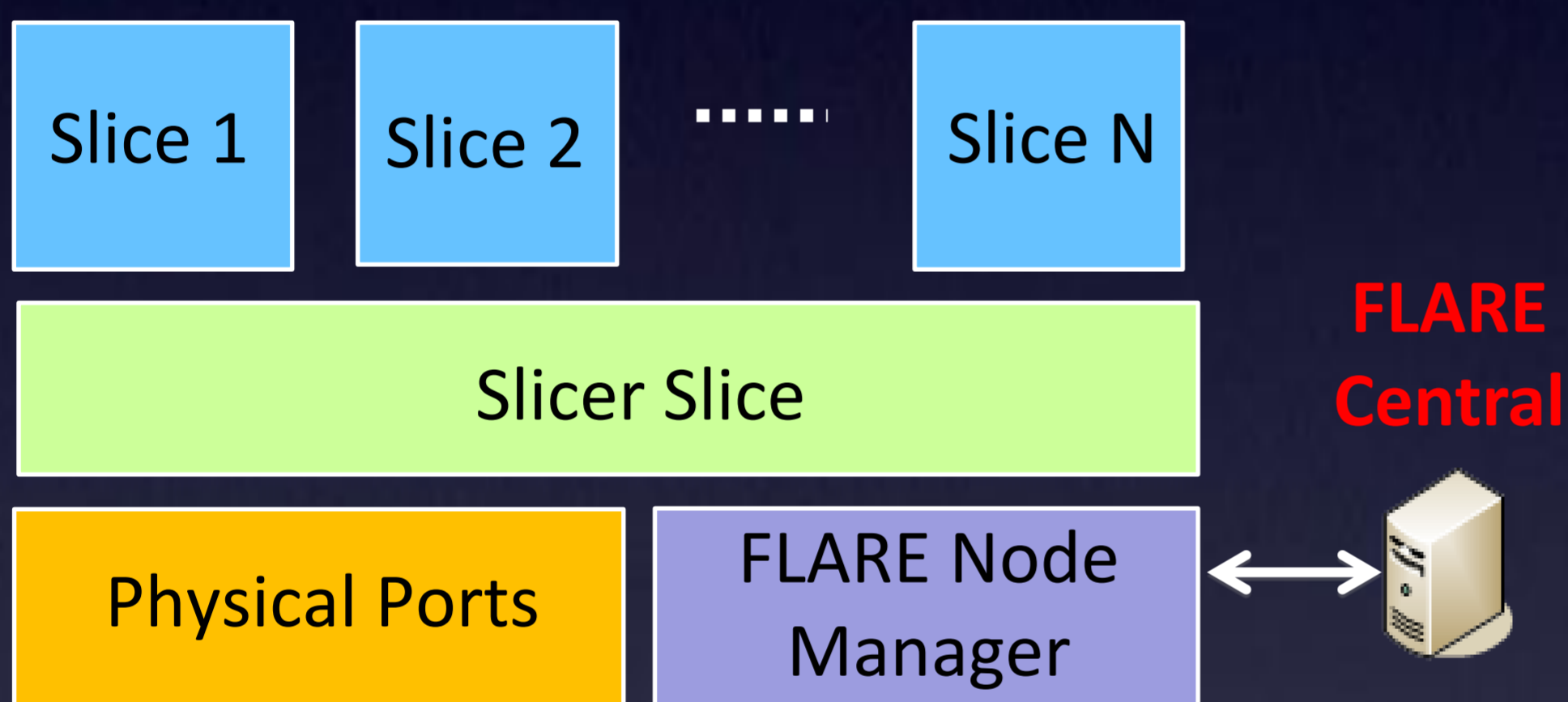
FLARE

Open Deeply Programmable Network Node Architecture

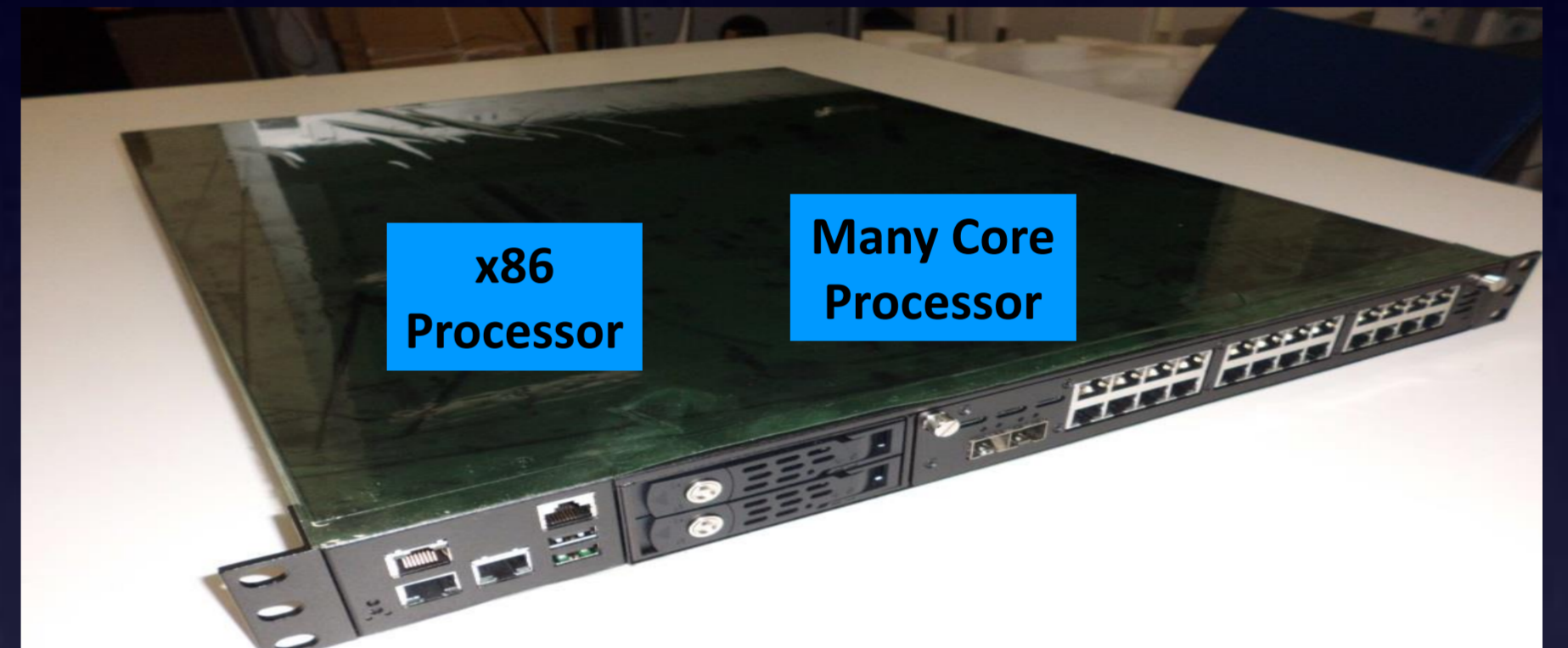
FLARE Node Development

FLARE Node Line Up

| | Hardware Configuration | Interfaces | Release |
|-------------------|------------------------|------------------------|---------|
| FLARE | Intel x86 TileGX36 | 4 x 10GbE | 2012 4Q |
| FLARE 2 | Intel x86 TileGX36 | 2 x10GbE and 8 x GbE | 2013 1Q |
| FLARE X | Intel x86 TileGX72 | 8 x 10GbE | 2013 4Q |
| FLARE 3 | Intel x86 TileGX72 | 2 x 10GbE and 24 x GbE | 2015 1Q |
| FLARE DPDK | Intel x86 (DPDK) | 2 to 8 x 10GbE | 2015 2Q |



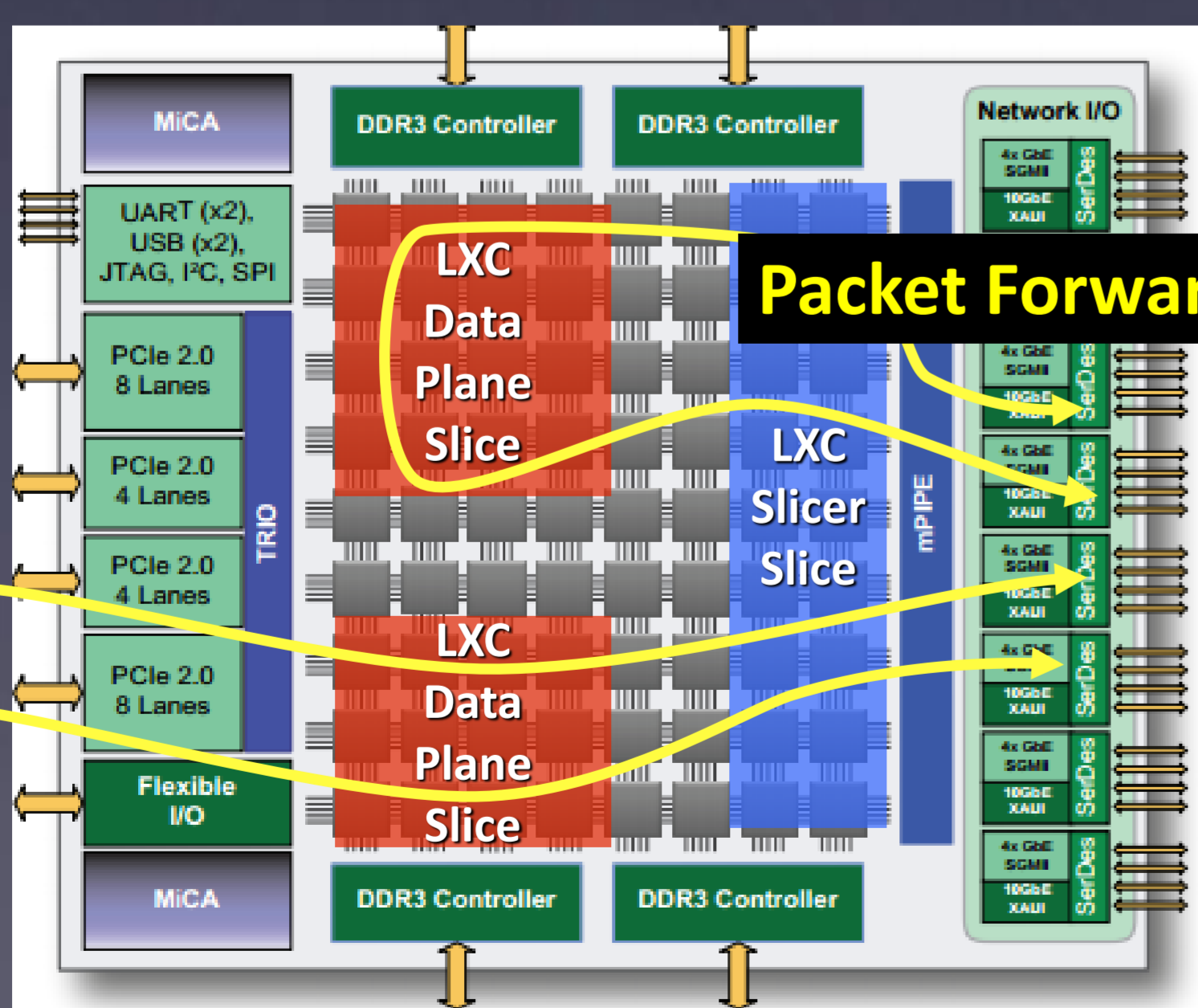
FLARE Node Architecture



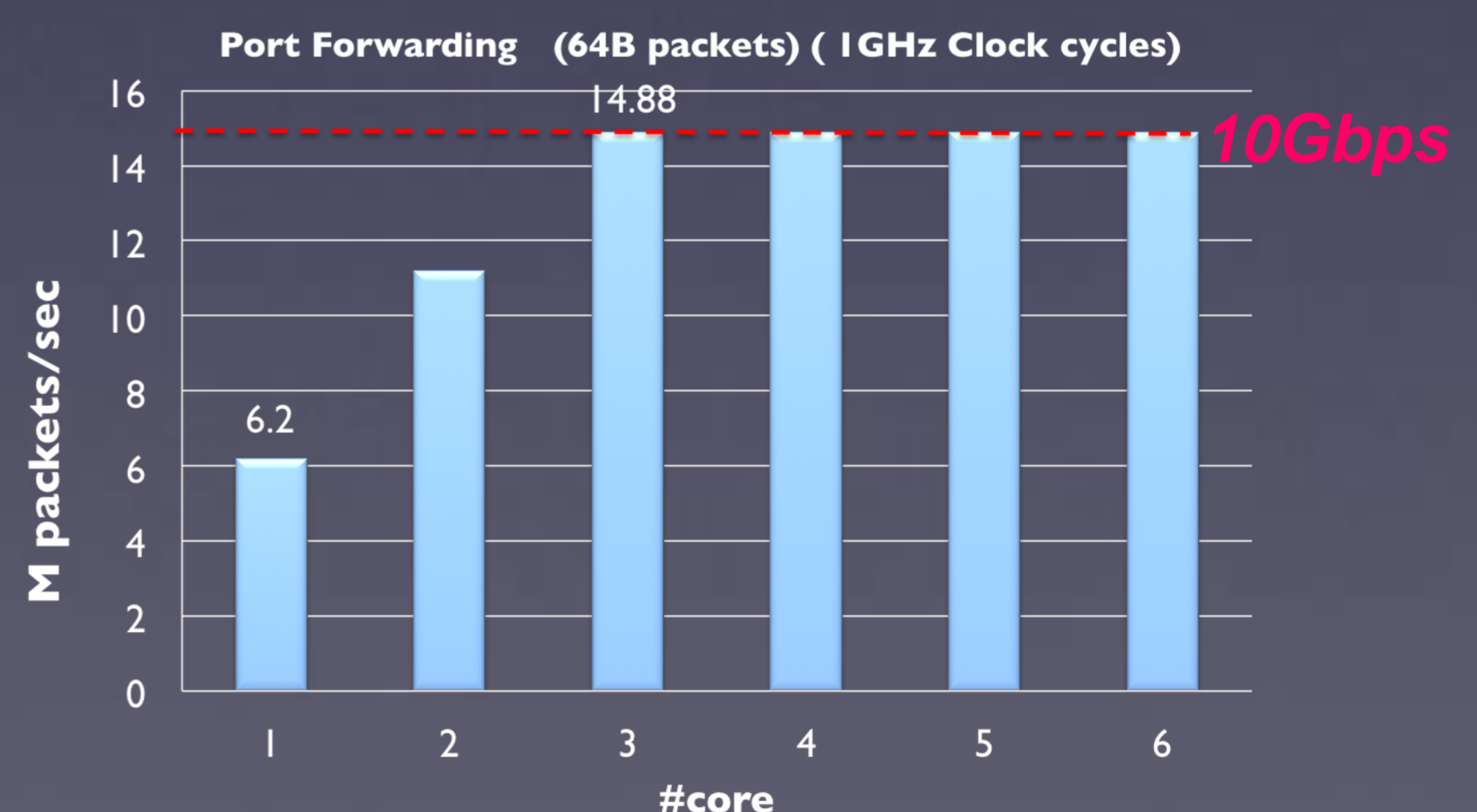
FLARE3 Node

| Features and Specifications | |
|-----------------------------|--|
| Control Plane | x86 CPU |
| Data Plane | 72 core EZ-Chip NPU |
| Ports | 24-port GbE and 2-port 10GbE SFP+ (or 8-port 10GbE SFP+) |
| Memory | Up to 128GB for NPU |
| Power | Redundant supply |
| Storage | Swappable SSD x2 |

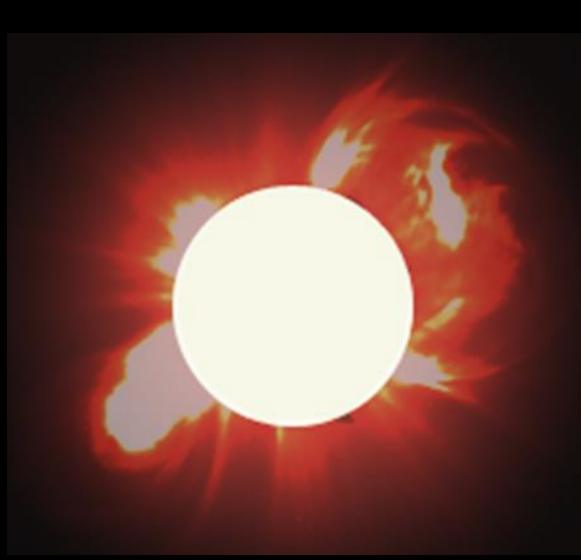
LXC: Linux Container on Zero Overhead Linux (ZOL)



Slice Architecture

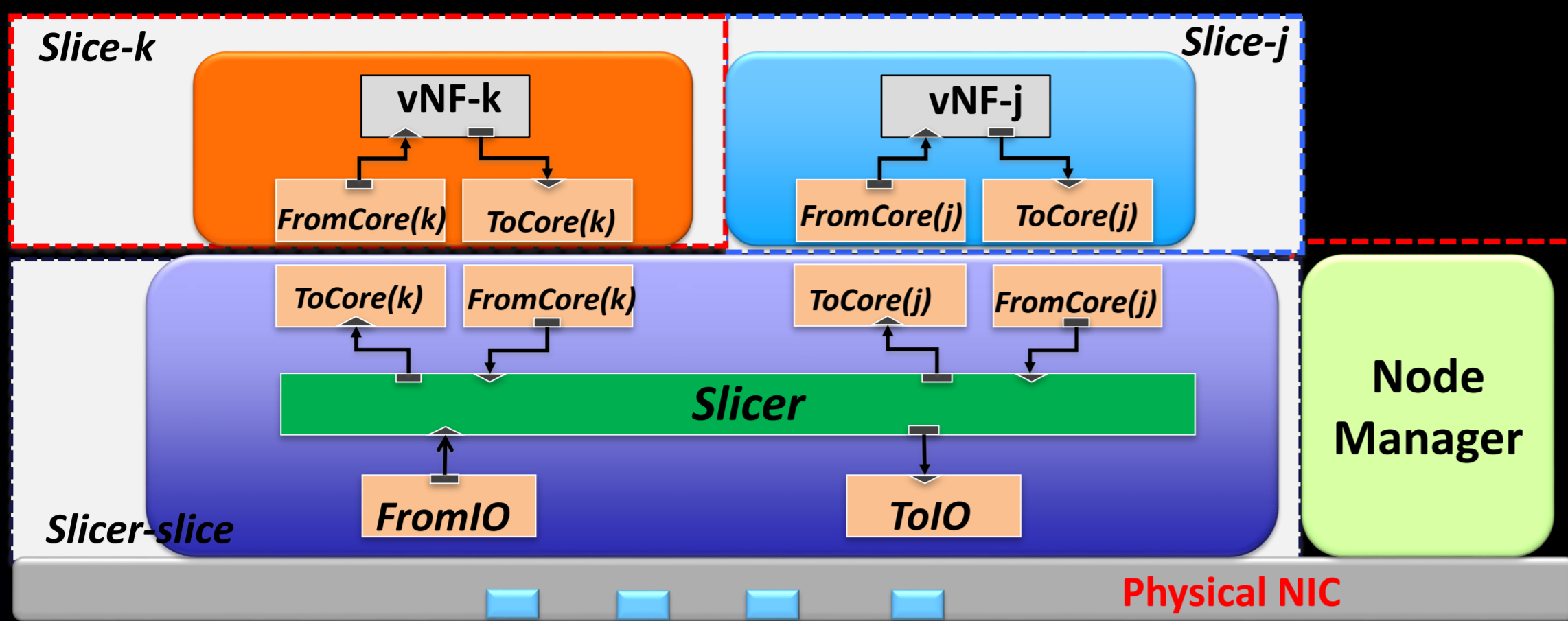


Packet I/O Performance



FLARE

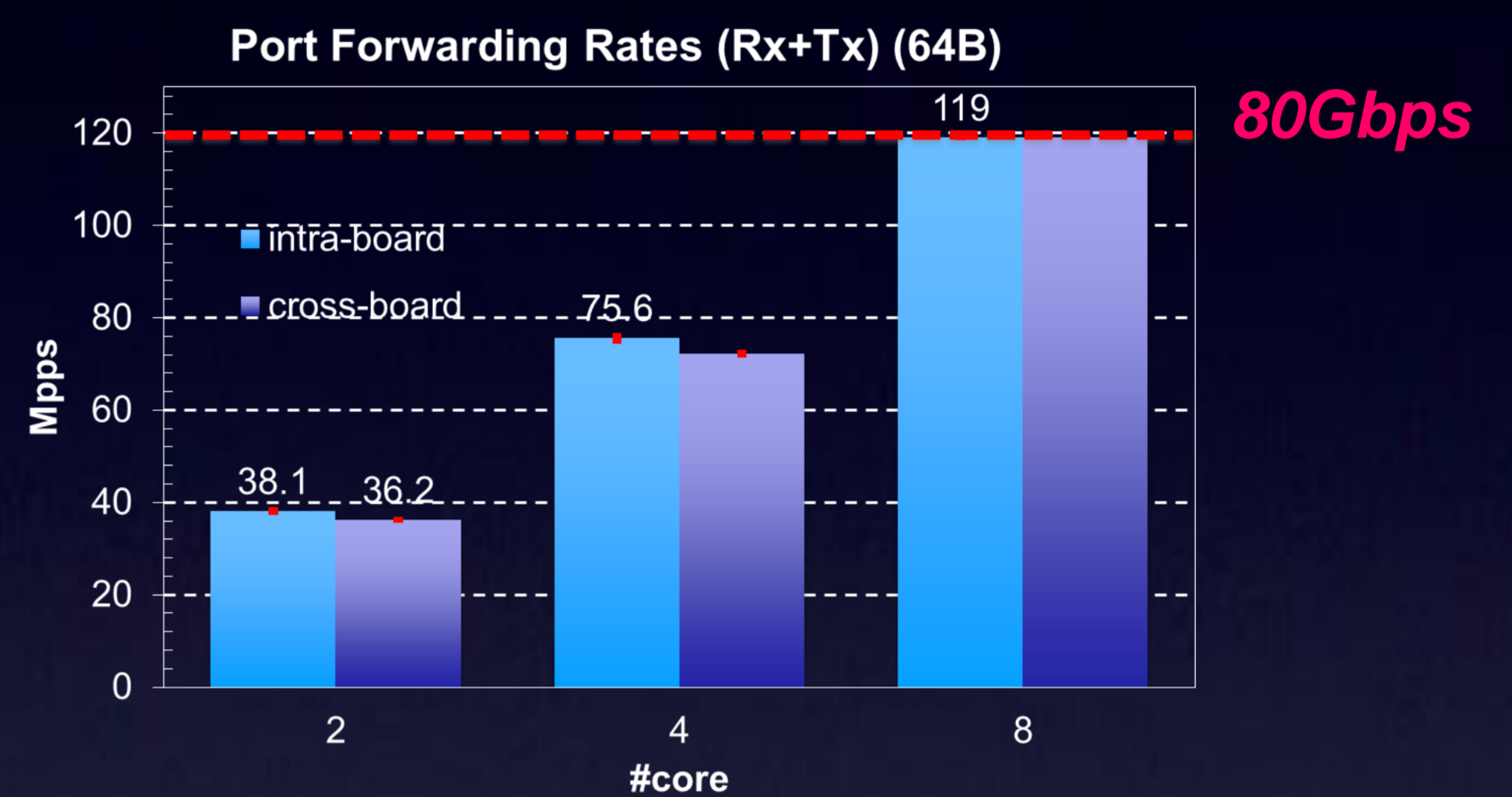
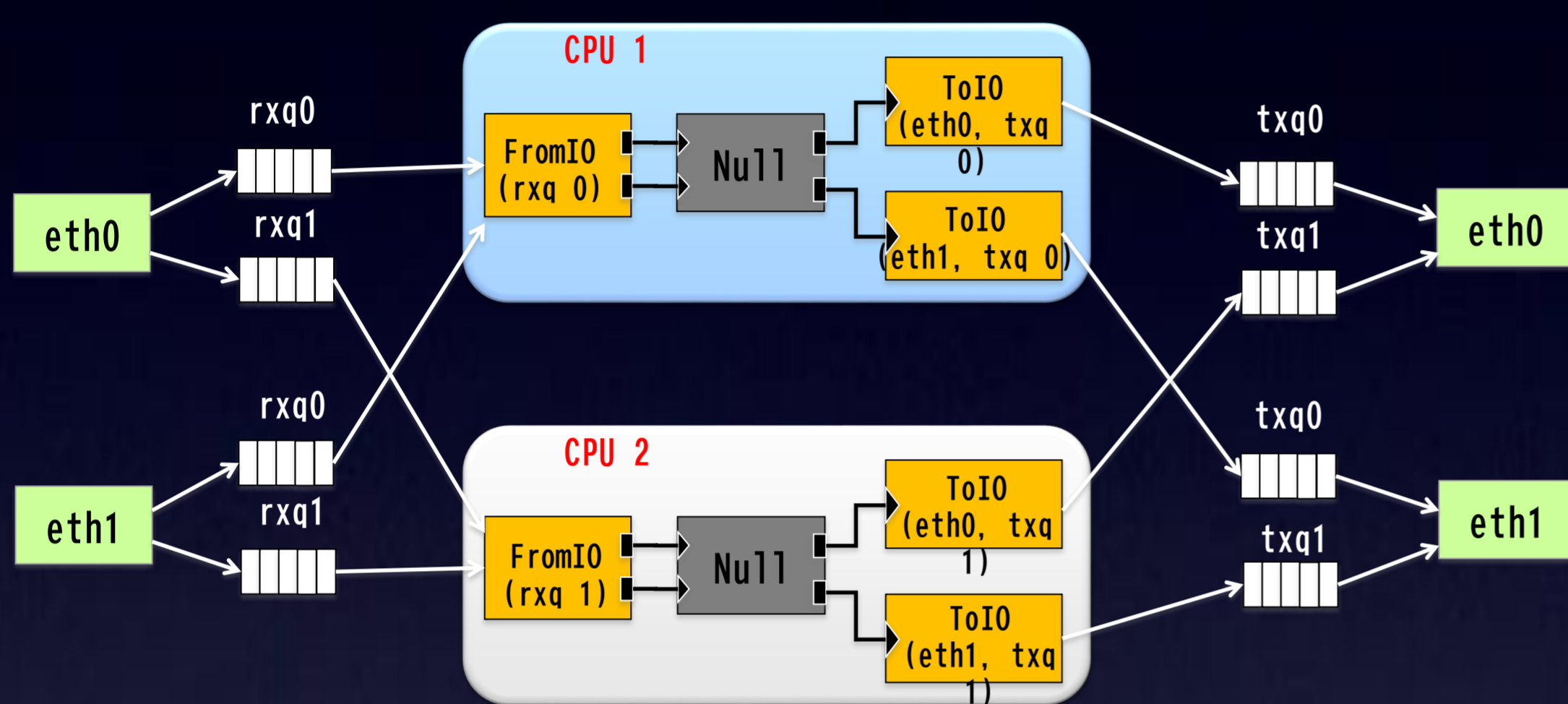
Open Deeply Programmable Network Node Architecture



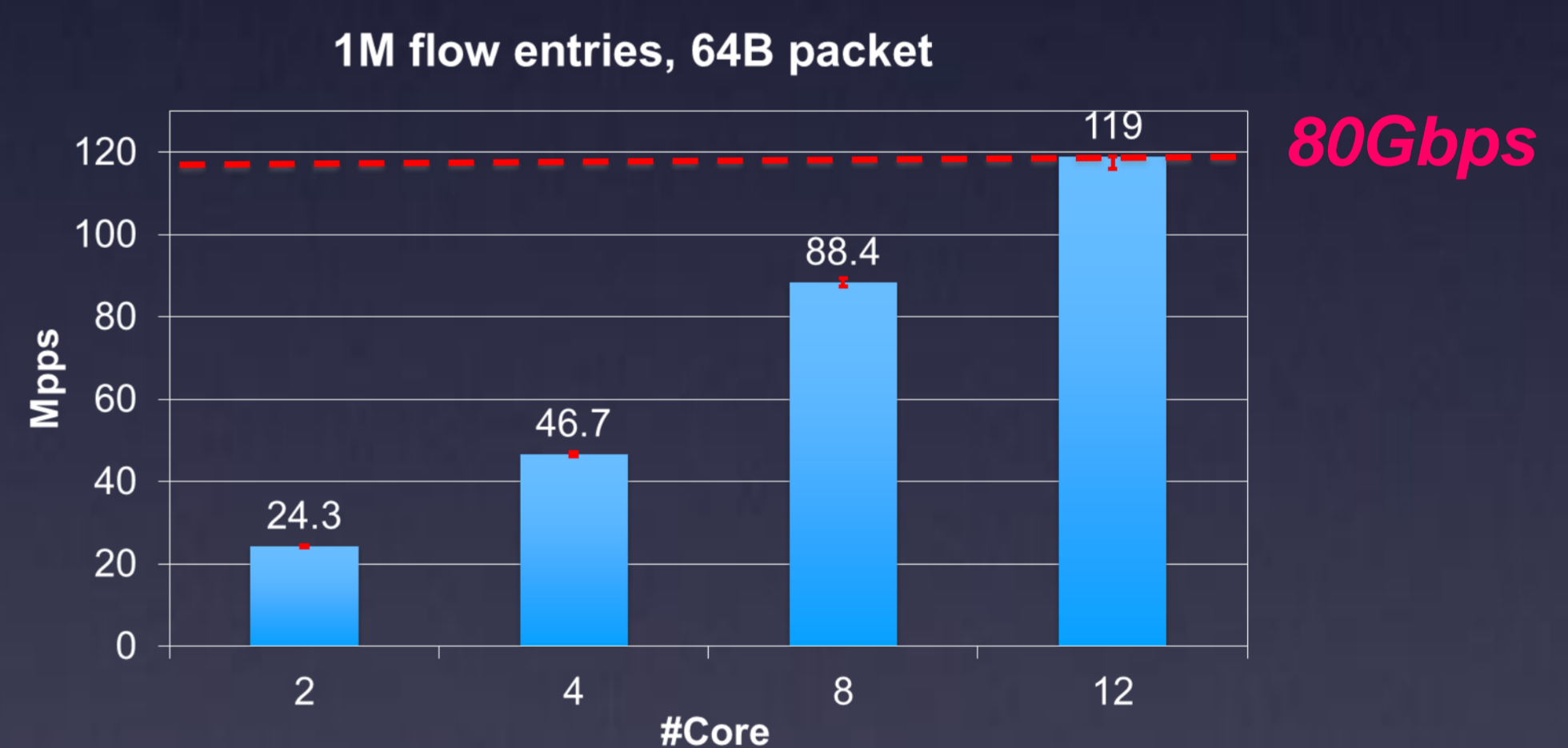
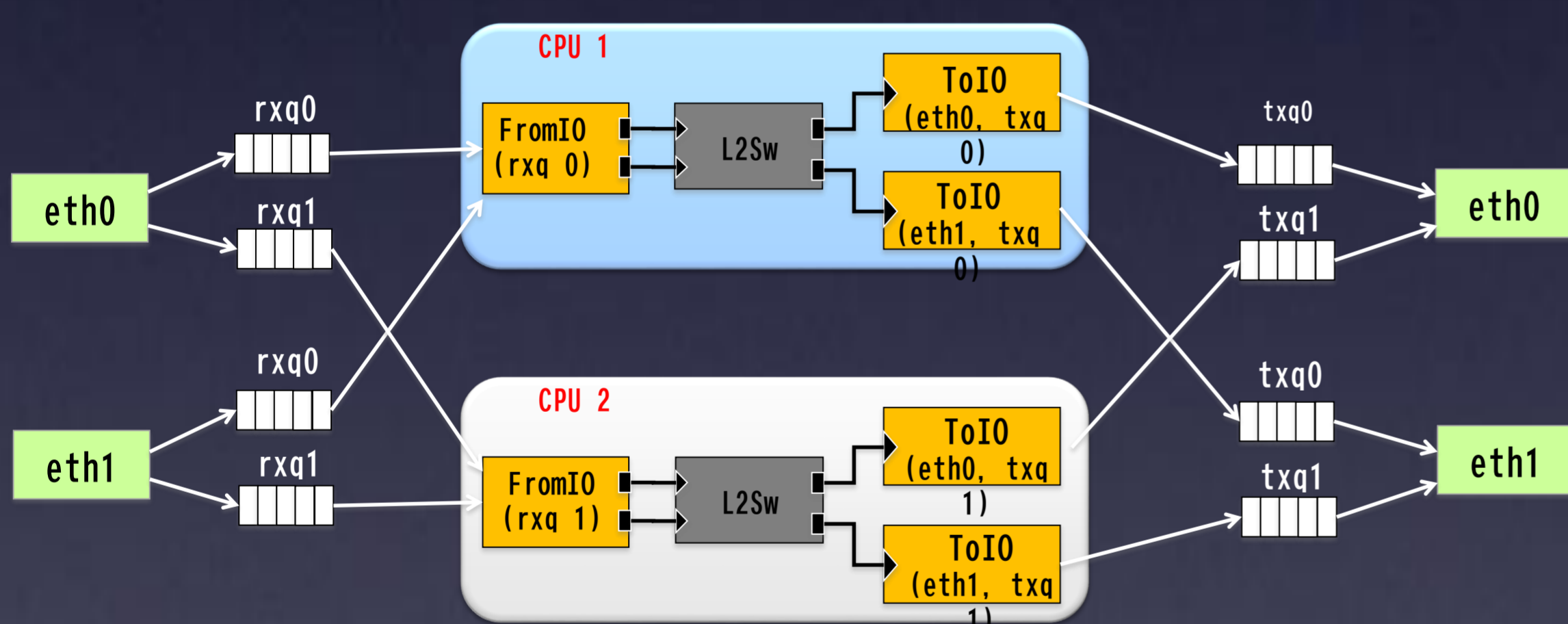
- Processor: two 10-core Intel Xeon E5-2687w v3@3.1GHz
- Memory: 16x16 GB DDR4
- Interface: two Intel X710 based quad-port 10GbE

FLARE DPDK Architecture

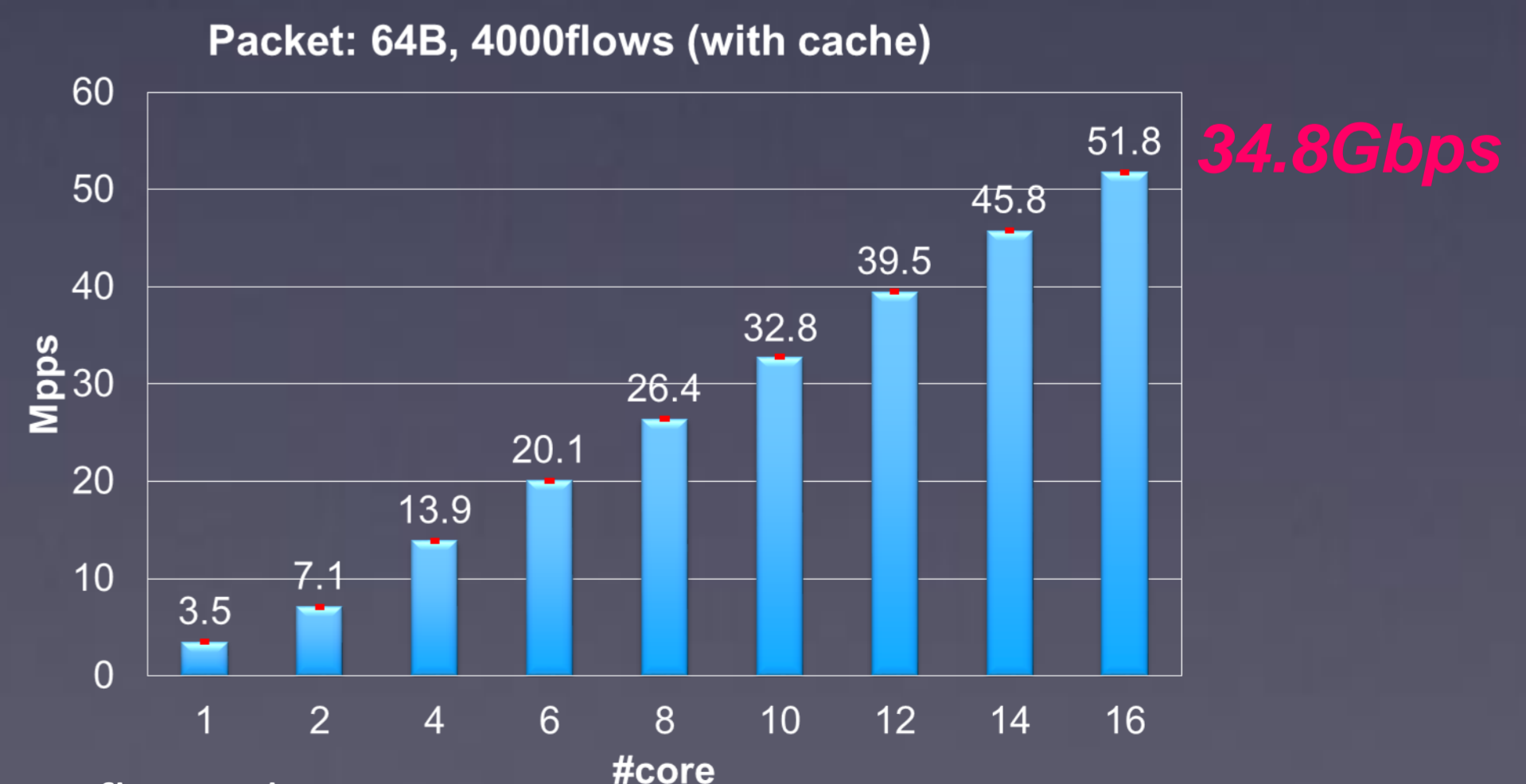
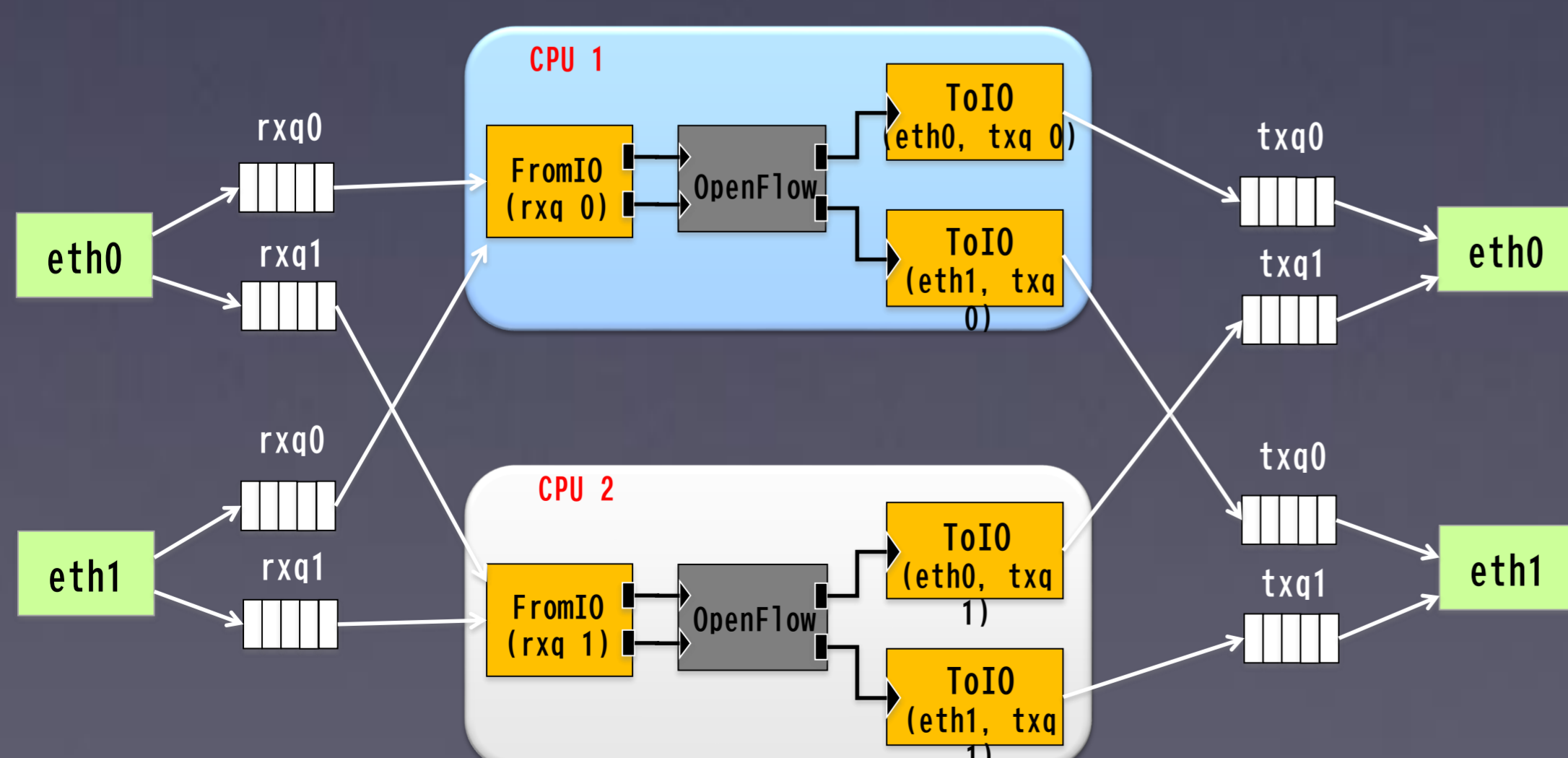
Port Forwarding



L2 Switch



OpenFlow 1.3



flow rules

- match: in_port=1, action: output=2
- match: in_port=2, action: output=1
- match: in_port=3, action: output=4
- match: in_port=4, action: output=3